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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/728,241	12/03/2003	Michael G. West	7293-105	7479

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EXAMINER	
PATEL, NITIN	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 03/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/728,241	WEST ET AL.	
	Examiner	Art Unit	
	Nitin Patel	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

I. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

II. Claims 1-26 are rejected under the judicially created doctrine of double patenting over claims 1-29 of U. S. Patent No. 6,683,604 B1 (West et al.,) since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows:

As per claim 1, West shows display system adapted to display input image data received one frame at a time at an input frame rate and an input resolution on a display having an output frame rate and an output resolution, comprising:

a pixel packing circuit adapted to generate coded image data responsive to a failsafe enable signal, the coded image data being a compressed representation of the input image data; and a pixel packing circuit adapted to generate output image data

capable of being displayed on the display responsive to the failsafe enable signal by manipulating the coded image data (In Col.9 lines 12-26).

As per claim 2, West shows a memory adapted to store the coded image data (in Col.9 lines 51-53).

As per claim 3, West shows the pixel packing circuit includes 'an input terminal adapted to receive the input image data; and a logic circuit adapted to generate the coded image data by logically manipulating the input image data (In Col.9 lines 53-58).

As per claim 4, West shows the input image data includes a plurality of digital image signals and wherein the logic circuit includes a first adder adapted to generate a first adder signal by adding the plurality of digital image signals; a second adder adapted to generate a second adder signal by adding first and second portions of the first adder signal; a plurality of registers coupled to the second adder and each adapted to store sequential second adder signals; and a first plurality of comparators adapted to generate a plurality of pixel bits by comparing the second adder signal to a first threshold limit; a second plurality of comparators adapted to compare the second adder signal to a second threshold limit; and a logic gate adapted to generate a palette bit by logically manipulating signals output from the second plurality of comparators (in Col.9 lines 28-50).

As per claim 5, West shows the first and second threshold limits are programmable (In Col.10 lines 61-62).

As per claim 6, West shows the plurality of digital image signals include RGB image signals (In Col.10 lines 63-64).

As per claim 7, West shows the plurality of registers includes as many registers as there are bits in the second adder signal (In Col.10 lines 65-67).

As per claim 8, West shows the pixel unpacking circuit includes a multiplexer circuit adapted to generate the output image data responsive to a pixel select signal (In Col. 9 lines 59-61).

As per claim 9, West shows the coded image data includes a plurality of pixel bits and a palette bit and wherein the multiplexer circuit includes a multiplexer and a logic gate, the multiplexer selecting one of the pixel bits responsive to the pixel select signal and the logic gate generating a logic gate output signal by logically manipulating the selected pixel bit and the palette bit (In Col.9 lines 62-67).

As per claim 10, West shows the failsafe enable signal includes a first and second logic states, the first logic state indicating that the input frame rate exceeds the output frame rate (in Col.10 lines 6-9).

As per claim 11, West shows input image signals provided to the system one frame at a time, the input image signals having input characteristics; a display capable of displaying output image signals having output characteristics; a failsafe enable adapted to identify when the input characteristics exceeds the output characteristics; a packing circuit adapted to generate a coded signal by compressing the input image signals responsive to the failsafe enable, a memory adapted to store the coded signal; and an unpacking circuit adapted to generate the output image signals at the output characteristics by logically manipulating the coded signal responsive to the failsafe enable (In Col.10 lines 25-35).

As per claim 12, West shows the input characteristics include an input frame rate and an input resolution and wherein the output characteristics include an output frame rate and an output resolution (In Col.10 lines 10-15).

As per claim 13, West shows the coded signal includes a plurality of pixel bits and a palette bit and wherein the packing circuit includes: a first adder adapted to generate a first adder signal by adding the input image signals; a second adder adapted to generate a second adder signal by adding first and second portions of the first adder signal; a plurality of serially connected registers coupled to the second adder, each register being adapted to store sequential second adder signals; and a first plurality of comparators adapted to generate the plurality of pixel bits by comparing the second adder signal to a first threshold; a second plurality of comparators adapted to generate a corresponding plurality of comparator signals by comparing the second adder signal to a second threshold; and a logic gate adapted to generate the palette bit by logically manipulating the plurality of comparator signals (in Col.10 lines 39-60).

As per claim 14, West shows the coded signal includes a plurality of pixel bits and a palette bit and wherein the unpacking circuit includes: a multiplexer adapted to select one of the plurality of pixel bits; and a logic circuit adapted to logically manipulate the selected pixel bit with the palette bit (In Col.9 lines 62-67).

As per claim 15, West shows the input image signals include RGB signals representative of a color image and wherein the output image signals represent a gray scale version of the color image (In col. 10 lines 63-64).

As per claim 16,West shows an input pixel formatter circuit adapted to receive input signals at an input frame rate and an input resolution representative of an image and adapted to generate a coded signal representing a compressed version of the image responsive to a failsafe enable, a memory buffer adapted to store the coded signal; and a pixel value generator circuit adapted to generate output signals by manipulating the coded signals and providing the output signals to a display at an output frame rate and an output resolution responsive to the failsafe enable (In col. 12 lines 34-49).

As per claim 17, West shows a first adder adapted to generate a pixel bit intensity signal by digitally adding the input signals; a second adder adapted to generate a pixel bit upper intensity signal by adding a first portion of the pixel bit intensity signal to a second portion of the pixel bit intensity signal; a plurality of registers adapted to store sequential upper bit intensity signals; and a first plurality of comparators adapted to generate the plurality of pixel bits by comparing corresponding upper bit intensity signals stored in the plurality of registers to a first threshold; a second plurality of comparators adapted to generate a corresponding plurality of comparator signals by comparing corresponding upper bit intensity signals stored in the plurality of registers to a second threshold; and a logic circuit adapted to generate the palette bit by logically manipulating the plurality of comparator signals (Incol.12 lines 50-67).

As per claim 18, West shows the first and second thresholds are Programmable (In col.13 lines 38-39).

As per claim 19, West shows there are as many registers in the plurality of registers as there are pixel bits in the plurality of pixel bits (In col.13 lines 40-43).

As per claim 20, West shows the input signals are RGB color signals and wherein the output signals are a gray scale version of the RGB color signals (In col.13 lines 43-45).

As per claim 21, West shows in the coded signal represents a compression of a plurality of RGB signals (In col.13 lines 46-47).

As per claim 22, West shows the pixel value generator circuit comprises: a multiplexer adapted to select one of the plurality of pixel bits; and a logic circuit adapted to logically manipulate the selected pixel bit with the palette bit (In col.13 lines 47-51).

As per claim 23, West shows displaying digital image data having an input frame rate on a display having an output frame rate, comprising enabling a failsafe signal if the input frame rate exceeds the output frame rate; compressing the image data responsive to the failsafe signal; displaying the compressed image data; and allowing a user to change display settings after displaying the compressed image data (In col.14 lines 3-14).

As per claim 24, West shows compressing the image data includes receiving RGB input signals at the input frame rate, the RGB signals being representative of a color image; generating a pixel intensity signal by summing the RGB signals; generating an upper pixel intensity signal by summing a first and second portion of the pixel intensity signal; repeating for a predetermined number of times receiving, generating a pixel intensity, and generating an upper pixel intensity; storing sequential upper pixel

intensity signals in a plurality of registers, generating a plurality of pixel bits by comparing the sequentially stored upper pixel intensity signals to a low threshold; comparing the sequentially stored upper pixel intensity signal to a high threshold; and generating a palette bit by logically manipulating results of the comparing to the high threshold (In Col. 14 lines 15-34).

As per claim 25, West shows programming the low and high thresholds (InCol.14 lines 35-37).

As per claim 26, West shows the image data comprises: generating a coded signal with the plurality of pixel bits and the palette bit, the coded signal representing a plurality of image pixels; storing the coded signal in a memory; sampling the stored coded signal at a sampling rate; selecting a pixel bit from the coded signal at the output frame rate; logically manipulating palette bit with the selected pixel bit at the output frame rate (In col. 14 lines 40-49).

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application

being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

2. Claims 1-3,8-10,11-12,14-15,16,23 is rejected under 35 U.S.C. 102(e) as being anticipated by Civanlar et al., U.S. Patent No. (5,691,768).

As per claims 1,11,12,16,23 Civanlar shows a display system adapted to display input data (In fig.1 element 101) received one frame at a time at an input frame rate and an input resolution on a display having an output frame rate and an output resolution (In col.6 lines 25-50) having a pixel packing circuit adapted to generate coded image data responsive to a failsafe enable signal (In col.9 lines38-45 and element 305 in fig.3), the coded image data being a compressed representation if the input image data (In col.7 lines 53-67) and a pixel unpacking circuit adapted to generate output image data capable of being displayed on the display responsive to the failsafe enable signal by manipulating the coded image data(as a encoded image data In col.8 lines 17-35).

As per claim 2, Civanlar shows a memory adapted to store the coded image data (In col.7 lines 25-27).

As per claim 3, Civanlar shows an input image signal and a logic circuit adapted to generate the coded image data by manipulating the image data (In col.6 lines 30-40 and In col.6 lines 58-61 element 106 as a logic circuit).

As per claims 8,9,14,15 Civanlar shows a multiplexer circuits to generate the output image data (In Col.13 lines 37 processing means to multiplexing slices or image

data) and a logic gate to manipulating the selected pixel bit and the palette bit (In col.10 lines 39-67).

As per claim 10, Civanlar shows enables first and second logic levels, the first logic state indicating the input frame rate exceeds the output frame rate (in Col.7 lines 25-52).

Allowable Subject Matter

3. Claims 4-7,13,17-22,24-26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reason for the indication of allowable subject matter:

The prior art fails to teach or suggest the input image data includes a plurality of digital image signals and wherein the logic circuit includes a first adder adapted to generate a first adder signal by adding the plurality of digital image signals and a second adder adapted to generate a second adder signal by adding first and second portions of the first adder signal; a plurality of registers coupled to the second adder and each adapted to store sequential second adder signals and a first plurality of comparators adapted to generate a plurality of pixel bits by comparing the second adder signal to a first threshold limit; a second plurality of comparators adapted to compare the second adder signal to a second threshold limit and a logic gate adapted a palette bit by logically manipulating signals output from the second plurality of comparators as claimed in claims 4-7,13,17-22,24-26.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Patel whose telephone number is 571-272-7677. The examiner can normally be reached on 8:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin H Shalwala can be reached on 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NP

March 19, 2005

Amare Mengistu
Primary Examiner